1. A seal ring structure comprising:

a substrate;

a plurality of layers of metal lines formed overlying said substrate; and

a plurality of metal vias through intermetal dielectric layers between said layers of metal lines wherein said metal vias interconnect said metal lines and wherein said plurality of layers of interconnected metal lines forms a continuous seal ring around a die and wherein a first width of said metal lines at a corner of said die is wider than a second width of said metal lines at edges of said die.

2. The seal ring structure according to Claim 1 wherein said metal lines are parallel to said edges of said die and wherein said metal lines are sloped at said corner of said die so that said metal lines do not have a sharp corner.

3. The seal ring structure according to Claim 1 wherein said first width of said metal lines covers a portion of said corner.

4. The seal ring structure according to Claim 1 wherein said first width of said metal lines covers the whole of said corner.

5. The seal ring structure according to Claim 1 wherein one or more slots or holes are formed in said first width of said metal lines at said corner.

6. The seal ring structure according to Claim 1 wherein said first width is about 1.5 times said second width or greater.

7. The seal ring structure according to Claim 1 further comprising semiconductor device structures within said die wherein a first distance between said semiconductor device structures and a corner portion of said seal ring is smaller than a second distance between said semiconductor device structures and an edge portion of said seal ring.

8. The seal ring structure according to Claim 7 wherein all active semiconductor device structures in said die are located within said seal ring and wherein devices involved in temperature testing may be located outside of said seal ring.

9. A method of forming a seal ring structure comprising:

providing a substrate; and

forming a continuous metal seal ring on said substrate along a perimeter of a die wherein said metal seal ring encloses device structures

wherein said metal seal ring is parallel to said edges of said die and wherein said metal seal ring is sloped at said corner of said die so as not to have a sharp corner and

wherein said metal seal ring has a first width along said edges and wherein said metal seal ring has a second width at said corners and wherein said second width is wider than said first width.

10. The method according to Claim 9 wherein said first width of said metal line covers a portion of said corner.

11. The method according to Claim 9 wherein said first width of said metal line covers the whole of said corner.

12. The method according to Claim 9 wherein one or more slots or holes are formed in said first width of said metal line at said corner.

13. The method according to Claim 9 wherein said first width is about 1.5 times said second width or greater.

14. The method according to Claim 9 wherein device structures enclosed by said seal ring include all active device structures except for devices involved in temperature testing which may be located outside of said seal ring.

15. The method according to Claim 9 wherein said forming a continuous metal seal ring along a perimeter of a die comprises forming a plurality of layers of metal lines interconnected by vias through intermetal dielectric layers wherein said plurality of layers of metal lines forms said continuous metal seal ring around said die.

16. A semiconductor device comprising:

semiconductor device structures formed in and on a substrate; and

a seal ring enclosing said semiconductor device structures forming a single die wherein a first distance between said semiconductor device structures and a corner portion of said seal ring is smaller than a second distance between said semiconductor device structures and an edge portion of said seal ring.

17. The device according to Claim 16 wherein said semiconductor device structures include gate electrodes, source and drain regions, and a plurality of layers of interconnected conductive lines.

18. The device according to Claim 16 wherein said semiconductor device structures include all active devices of said semiconductor device except for devices used for temperature testing.

19. The device according to Claim 16 wherein said seal ring comprises:

a plurality of layers of metal lines formed on said substrate; and

a plurality of metal vias through intermetal dielectric layers between said layers of metal lines wherein said metal vias interconnect said metal lines wherein said plurality of layers of interconnected metal lines forms a continuous seal ring around said die.

20. The device according to Claim 19 wherein said interconnected metal lines are parallel to said edges of said die and wherein said interconnected metal lines are sloped at said corner of said die so that said interconnected metal lines do not have a sharp corner.

21. The device according to Claim 16 wherein said corner portion of said seal ring has a first width and wherein said edge portion of said seal ring has a second width wherein said first width is wider than said second width.

22. The device according to Claim 21 wherein said first width is about 1.5 times said second width or greater.

23. The device according to Claim 21 wherein said first width of said seal ring covers a portion of said corner portion of said seal ring.

24. The device according to Claim 21 wherein said first width of said seal ring covers the whole of said corner portion of said seal ring.

25. The device according to Claim 16 wherein one or more slots or holes are formed in said corner portion of said seal ring.